XRT83SL314/L314EVAL

EVALUATION SYSTEM USER MANUAL

EVALUATION KIT PART LIST

This kit contains the following:

- XRT83SL314/L314EVAL Application Board
- XRT83SL314/L314 GUI Evaluation Software
- XRT83SL314/L314 128-Pin TQFP
- XRT83SL314/L314EVAL User Manual
- XRT83SL314/L314 Datasheet

FEATURES

- CPLD Design Which Emulates Microprocessor Support for the 8-Bit Parallel Interface
- 25 DIN Connector for Easy Connection Through a Standard Parallel Port to a PC
- CD ROM or Floppy Disk Containing the GUI Software (Executable File)
- Line Interface Modules Coupled to the Receiver Inputs and Transmitter Outputs
- Power Supply Design Allowing a Single 3V Supply voltage
- Accessible I/O Interface for Common Laboratory Equipment
- Optimized layout with Six Layers

INTRODUCTION

The XRT83SL314/L314EVAL is a complete printed circuit board for characterizing Exar's XRT83SL314/L314. The XRT83SL314/L314 is a fully integrated fourteen channel, long haul, short haul line interface unit for T1, E1 or J1 applications.

This application board combines a proven PC board layout with optimized analog and digital interface circuitry. The XRT83SL314/L314EVAL contains the device being tested, CPLD for emulating microprocessor support for the parallel interface, line interface modules coupled to the receiver inputs and transmitter outputs, and I/O headers for a flexible user interface. Complete AC and DC performance of the XRT83SL314/L314 can be evaluated by interfacing external laboratory equipment.

SYSTEM CONFIGURATION-LAB SETUP

The XRT83SL314/L314EVAL application board is setup as a common test circuit. Figure 1 shows a simplified block diagram of the default test configuration.

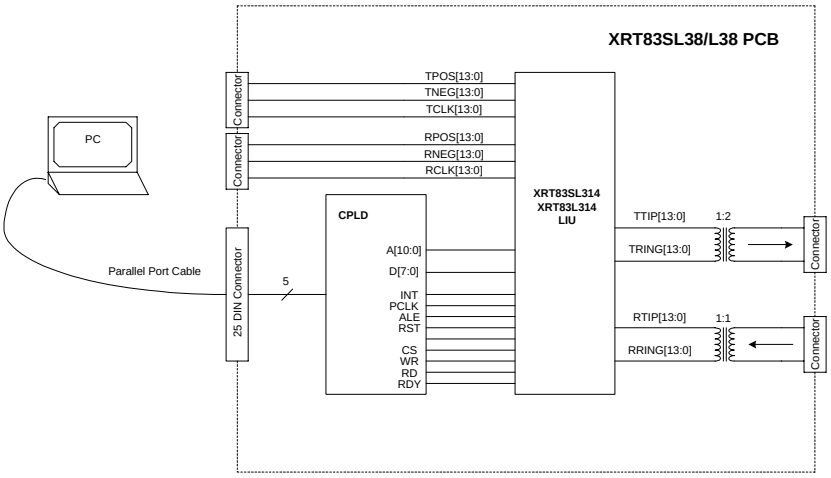


Figure 1 Simplified Block Diagram of the XRT83SL314/L314EVAL Application Board

APPLICATION CIRCUITRY

CPLD

The XRT83SL314/L314EVAL uses a CPLD designed to emulate a microprocessor support module for a parallel interface. Using Exar's GUI software (included in the evaluation kit), the XRT83SL314/L314EVAL can be controlled through a standard parallel port cable connected to a PC. The GUI was written to simplify the evaluation process of Exar's LIU. Access to all the control registers and functionality fo all fourteen channels is available. For information on the GUI software, see the "XRT83SL314/L314EVAL GUI SOFTWARE" section of this manual. Figure 2 is a simplified block diagram of the CPLD interface.

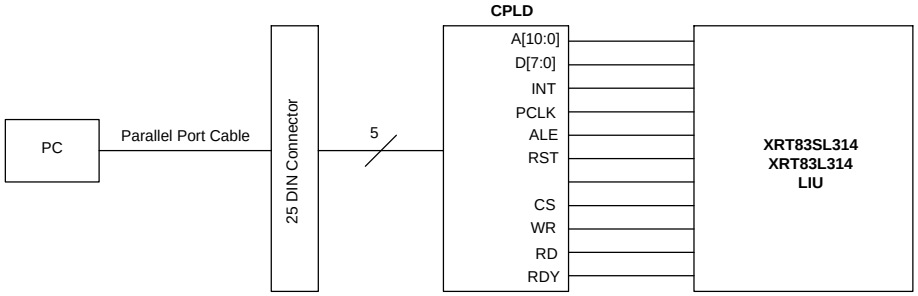


Figure 2 Simplified Block Diagram of the CPLD Interface

Line Interface Module

Internal Impedance

The XRT83SL314/L314 has the termination impedance inside the LIU. No termination resistors are necessary for the transmit outputs. This allows the user to have one bill of materials for all three applications. Figure 3 is a simplified block diagram of the interface connection.

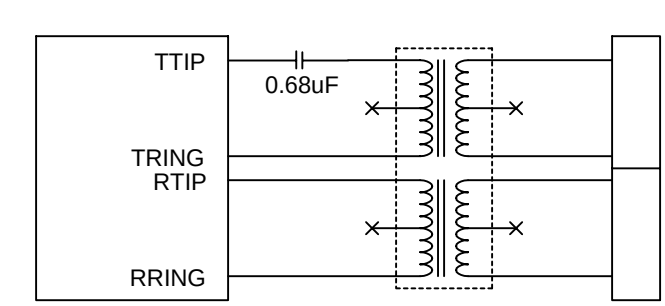


Figure 3 Simplified Block Diagram of the Interface Connection

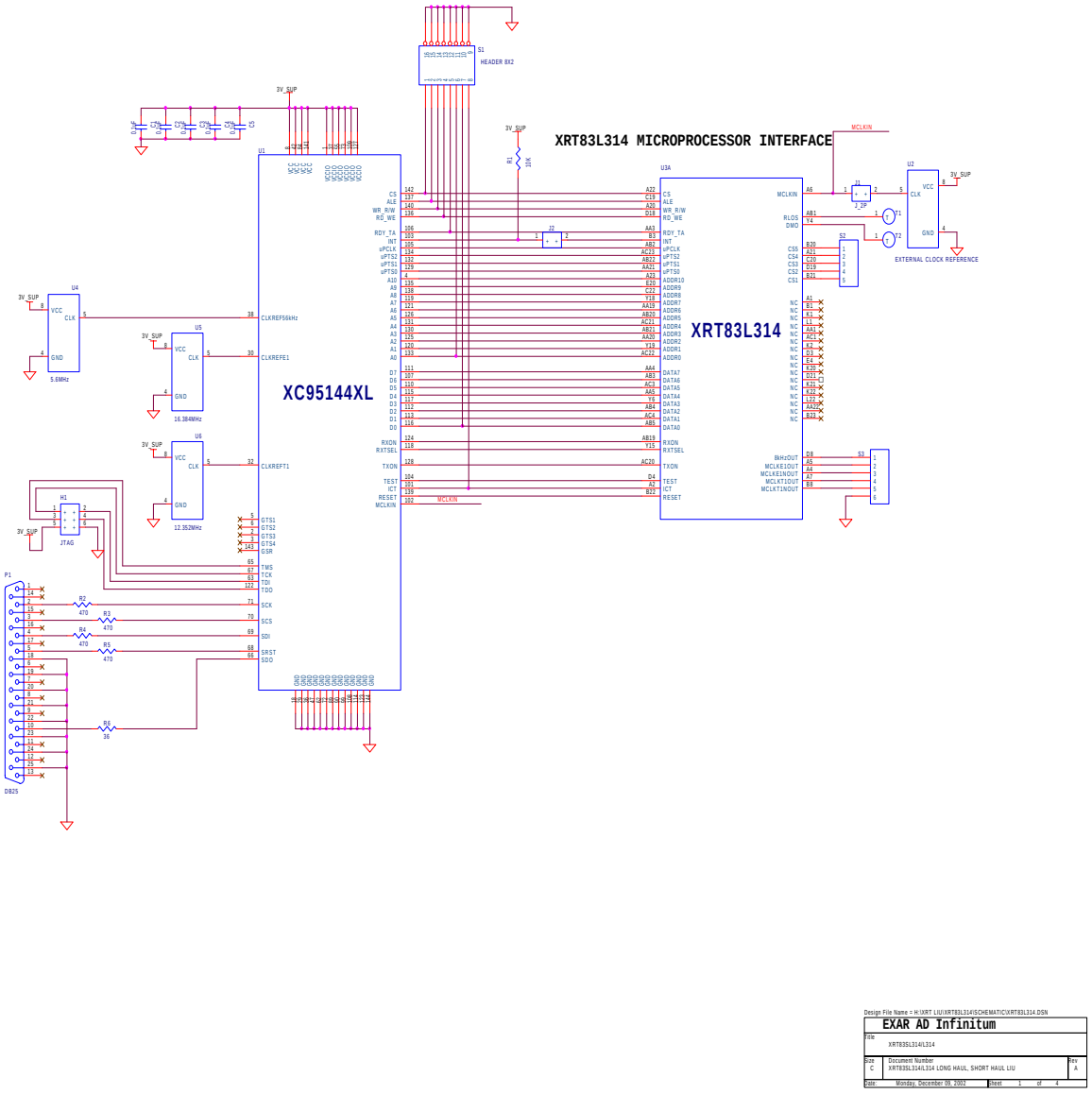


Figure 4 XRT83SL314/L314EVAL Schematic Page 1

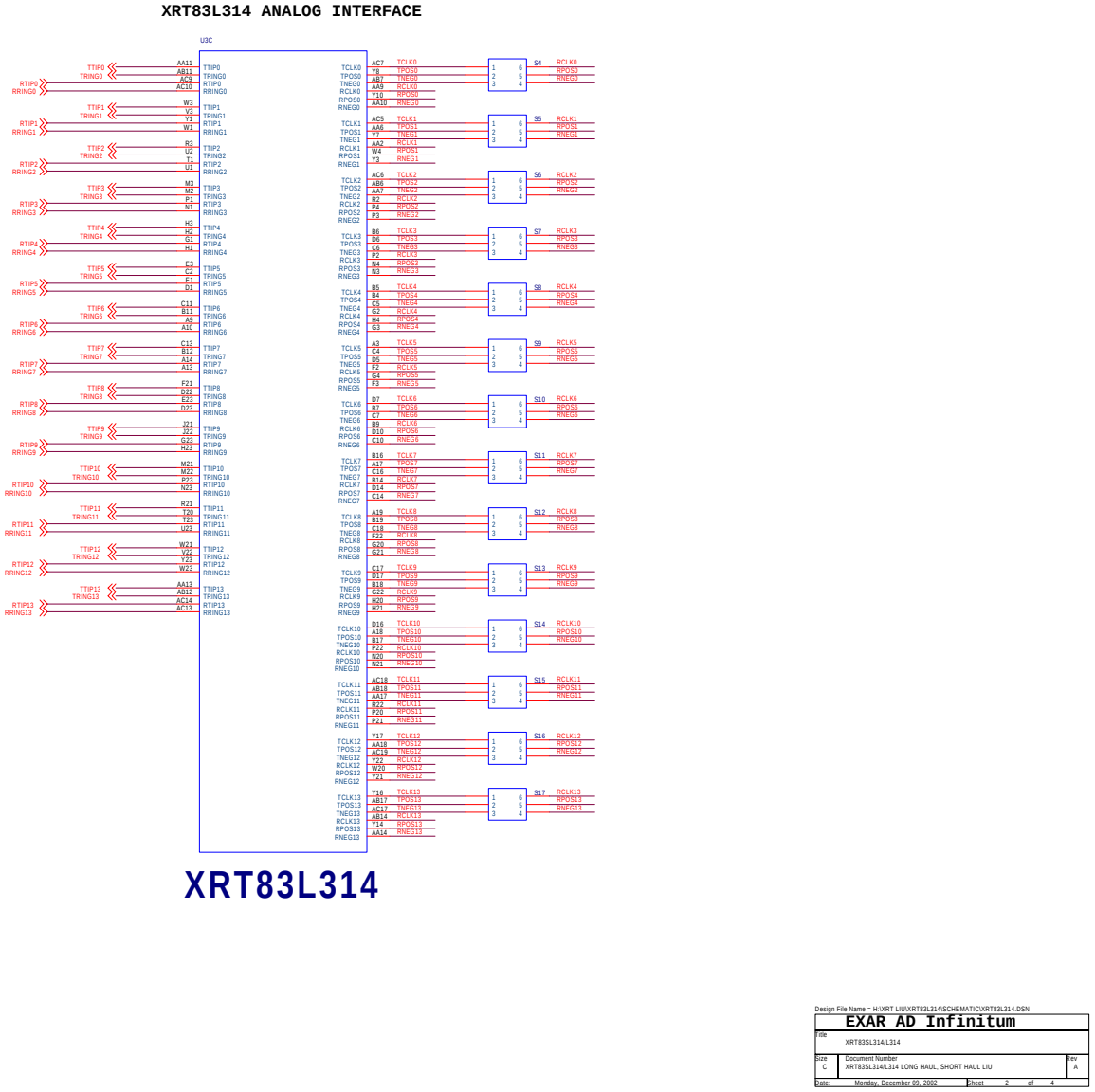
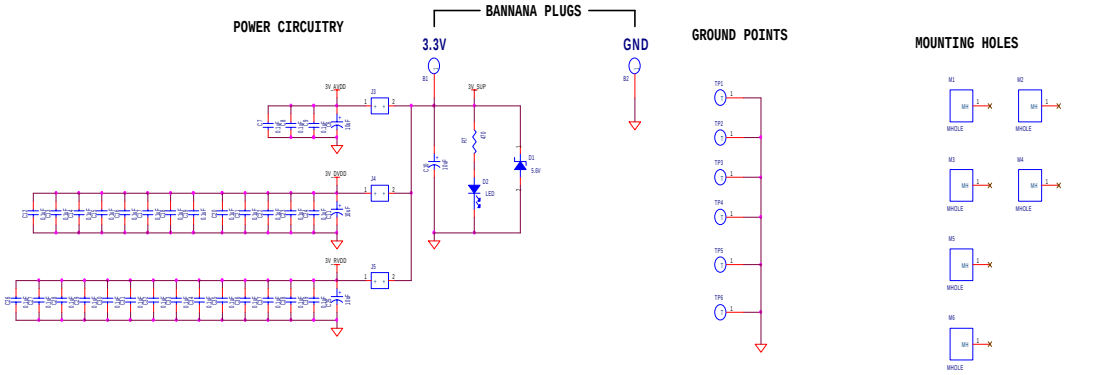
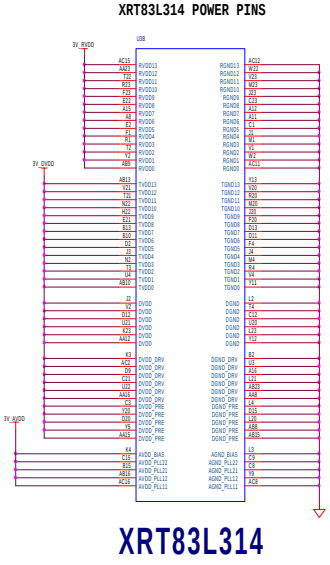


Figure 5 XRT83SL314/L314EVAL Schematic Page 2





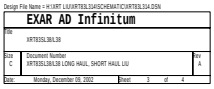


Figure 6 XRT83SL314/L314EVAL Schematic Page 3

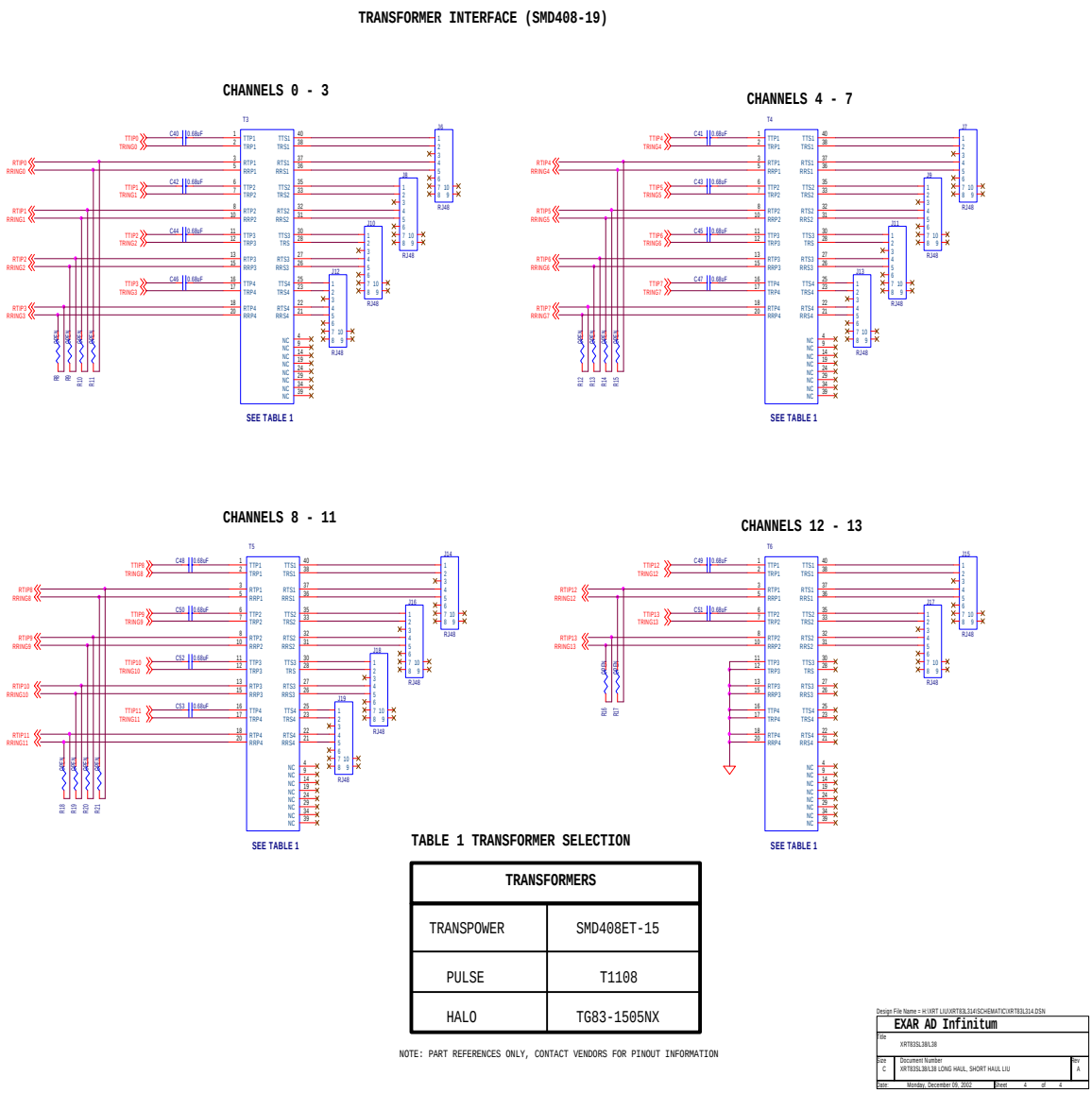


Figure 7 XRT83SL314/L314EVAL Schematic Page 4

Layout Recommendations

TVDD

Transmit Analog Power Supply (3.3V ±5%)

TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.

RVDD

Receive Analog Power Supply (3.3V ±5%)

For long haul applications, RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.

Note: In long haul applications where the receive inputs can be severely attenuated, it is critical to have a clean power supply design and clean PCB layout with respect to RVDD. It is highly recommended that RVDD be isolated from DVDD and TVDD.

DVDD

Digital Power Supply (3.3V ±5%)

DVDD should be isolated from the analog power supplies. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor.

AVDD

Analog Power Supply (3.3V ±5%)

AVDD should be isolated from the digital power supplies. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1µF capacitor.

GND

It's recommended that all ground pins of this device be tied together at one common ground point.